WHAT IS CLAIMED IS:

1. A latch circuit comprising:

a sample section activated during a sample period by a sample signal to sample a pair of complementary data signals, to deliver said complementary data signals through a pair of sample output nodes;

a latch section activated during a hold period by a hold signal to latch said complementary data signals through said sample output nodes, to deliver said complementary data signals through a pair of latch output nodes, said sample signal and said hold signal occurring alternately with each other; and

a precharge section for precharging said latch output nodes during said sample period.

2. The latch circuit according to claim 1, wherein:

said latch section includes first and second inverters for receiving said complementary data signals through said sample output nodes, and a latch-section activating circuit for activating said first and second inverters during said hold period;

said first inverter includes a first transistor having a gate connected to one of said sample output nodes and connected between a high-potential power source line and one of said latch output nodes, a second transistor connected between said one of said latch output nodes and the other of said sample output nodes and being OFF during said sample period, and a third transistor having a gate connected to the other of said latch output nodes

and connected between said other of said sample output nodes and a low-potential power source line; and

said second inverter includes a fourth transistor having a gate connected to said other of said sample output nodes and connected between said high-potential power source line and said other of said latch output nodes, a fifth transistor connected between said other of said latch output nodes and said one of said sample output nodes and being OFF during said sample period, and a sixth transistor having a gate connected to said one of said latch output nodes and connected between said one of said sample output nodes and said low-potential power source line.

3. The latch circuit according to claim 2, wherein said latch-section activating circuit includes a seventh transistor connected between said third transistor and said low-potential power source line and being ON during said hold period, and an eighth transistor connected between said sixth transistor and said low-potential power source line and being ON during said hold period.

4. The latch circuit according to claim 2, wherein said latch-section activating circuit includes a seventh transistor connected between a node connecting said third transistor and said sixth transistor in common and said low-potential power source line and being ON during said hold period.

5. The latch circuit according to claim 2, wherein:

said sample section includes first and second data signal input

blocks;

said first data signal input block includes seventh and eight transistors connected in series between said high-potential power source line and said one of said sample output nodes, said seventh transistor having a gate receiving one of said complementary data signals, said eighth transistor being ON during said ample period, and ninth and tenth transistors connected in series between said low-potential power source line and said one of said sample output nodes, said ninth transistor having a gate receiving the other of said complementary data signals, said tenth transistor being ON during said sample period; and

said second data signal input block includes eleventh and twelfth transistors connected in series between said high-potential power source line and said other of said sample output nodes, said eleventh transistor having a gate receiving said other of said complementary data signals, said twelfth transistor being ON during said sample period, and thirteenth and fourteenth transistors connected in series between said low-potential power source line and said other of said sample output nodes, said thirteenth transistor having a gate receiving said one of said complementary data signals, said fourteenth transistor being ON during said sample period.

6. The latch circuit according to claim 2, wherein:

said sample section includes first and second data signal input blocks, and a sample-section activating block for activating said first and second data signal input blocks during said sample period;

said first data signal input block includes seventh transistor

connected between said high-potential power source line and said one of said sample output nodes and having a gate receiving one of said complementary data signals, and an eighth transistor connected between said low-potential power source line and said one of said sample output nodes and having a gate receiving the other of said complementary data signals; and

said second data signal input block includes ninth transistor connected between said high-potential power source line and said other of said sample output nodes and having a gate receiving said other of said complementary data signals, and a tenth transistor connected between said low-potential power source line and said other of said sample output nodes and having a gate receiving said one of said complementary data signals.

7. The latch circuit according to claim 6, wherein said sample-section activating block includes an eleventh transistor connected in series with said seventh transistor between said high-potential power source line and said one of said sample output nodes and being ON during said sample period, a twelfth transistor connected in series with said eighth transistor between said low-potential power source line and said one of said sample output nodes and being ON during said sample period, a thirteenth transistor connected in series with said ninth transistor between said high-potential power source line and said other of said sample output nodes and being ON during said sample period, and a fourteenth transistor connected in series with said tenth transistor between said low-potential power source line and said other of said sample output nodes and being ON during said

sample period.

8. The latch circuit according to claim 6, wherein said sample-section activating block includes an eleventh transistor connected between a node connecting said seventh transistor and said ninth transistor in common and said high-potential power source line and being ON during said sample period, and a twelfth transistor connected between a node connecting said eighth transistor and said tenth transistor in common and said low-potential power source line and being ON during said sample period.